

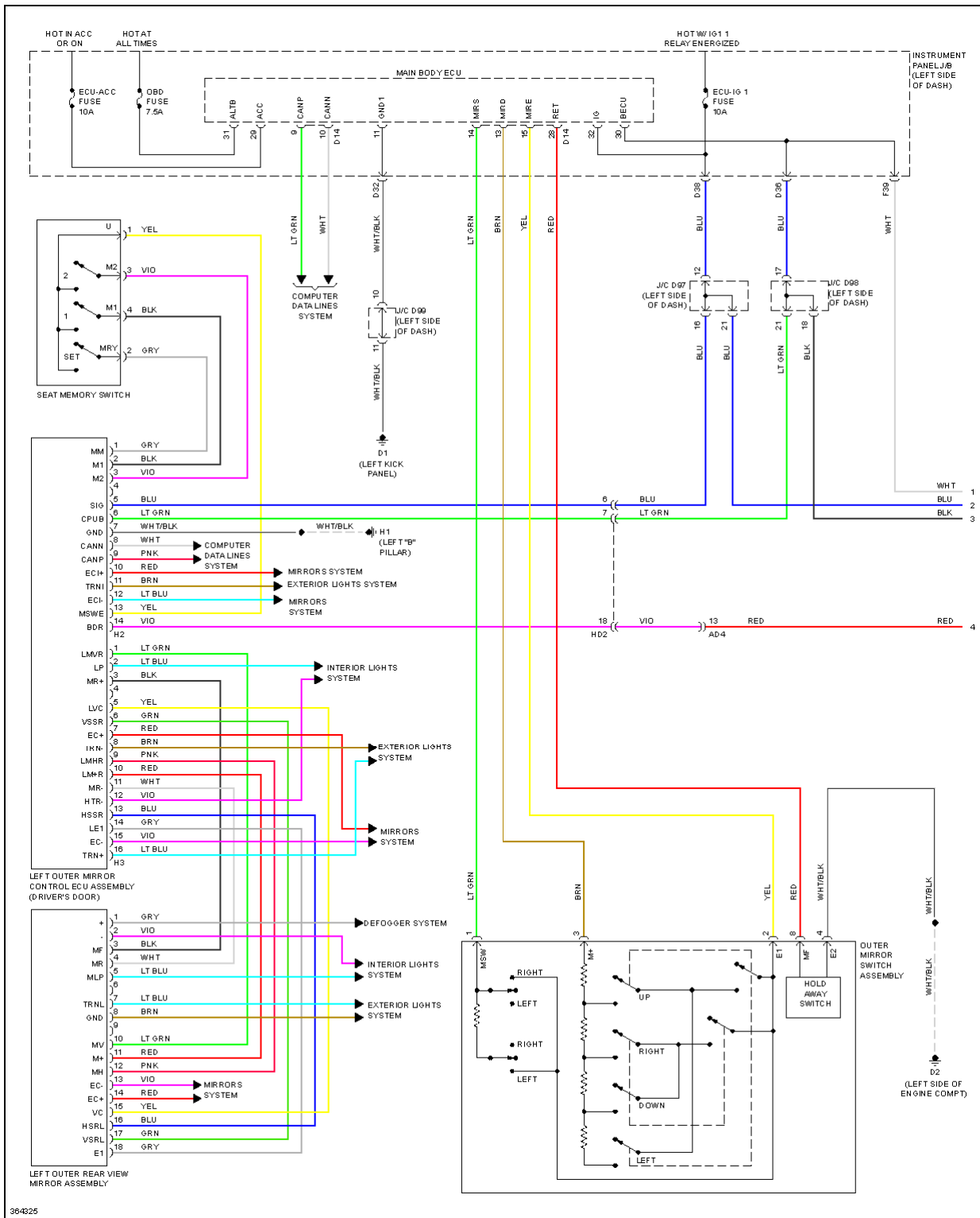


Fig. 57: Memory Mirrors Circuit (1 of 2)

